PVP 20

Code: 20EC4501B

III B.Tech - I Semester – Regular / Supplementary Examinations
NOVEMBER 2024

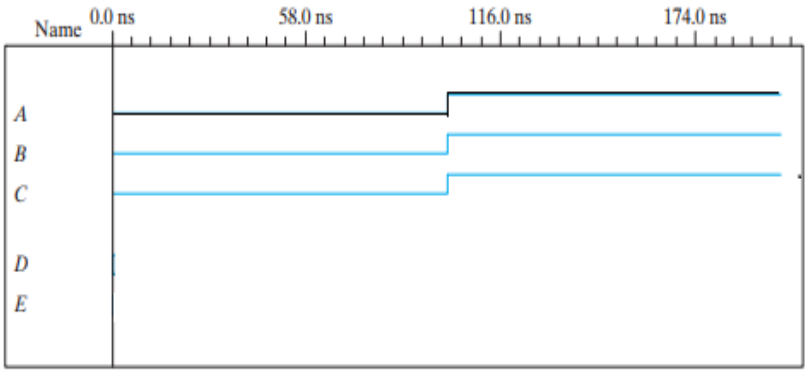
DIGITAL INTEGRATED CIRCUITS & APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
UNIT-I					
1	a)	Draw the typical VLSI Design flow and explain about it.	L2	CO1	7 M
	b)	Explain about instantiation in Verilog HDL with an example.	L2	CO1	7 M
OR					
2		Explain different Verilog data types and operators.	L2	CO1	14 M
UNIT-II					
3	a)	Write a Verilog Data Flow model to implement Full Adder.	L2	CO2	7 M
	b)	Draw the Timing Waveforms of the output ports D, E for the following Verilog HDL Program.	L2	CO2	7 M

		module delay1(A, B, C, D, E); output D, E; input A, B, C; wire w1; and #(30) G1 (w1, A, B); not #(10) G2 (E, C); or #(20) G3 (D, w1, E); endmodule The input excitation is shown below  			
		OR			
4	a)	Write a Verilog program to implement 2:1 Multiplexer using if-else statements.	L2	CO2	7 M
	b)	Explain the use of initial block and always block in the Verilog HDL.	L2	CO2	7 M
		UNIT-III			
5	a)	Explain the advantages of CMOS logic over other logic families.	L2	CO2	7 M
	b)	Design 2 input NOR gate in CMOS logic.	L3	CO2	7 M
		OR			

6	a)	Write short notes on CMOS/TTL Interface.	L2	CO2	7 M
	b)	Define Noise Margin and analyze CMOS inverter circuit.	L3	CO2	7 M
		UNIT-IV			
7	a)	Write a Verilog Gate-Level model for 2 to 4 Decoder.	L3	CO3	7 M
	b)	Develop the Verilog model for IC 74x138.	L3	CO3	7 M
		OR			
8	a)	Write a Verilog program for IC 74x151.	L3	CO3	7 M
	b)	Develop the Verilog model for IC 74x85.	L3	CO3	7 M
		UNIT-V			
9	a)	Develop Verilog model for IC 74x175.	L3	CO4	7 M
	b)	Write a Verilog behavioral program to implement IC 74x375.	L3	CO4	7 M
		OR			
10	a)	Write a Verilog Behavioral program to implement synchronous counter IC 74x93.	L3	CO4	7 M
	b)	Develop Verilog model for IC 74x74.	L3	CO4	7 M